FAIRCHILD SEMICONDUCTOR™

October 1986
Revised June 2001

DM74ALS646
Octal 3-STATE Bus Transceiver and Register

General Description

This device incorporates an octal bus transceiver and an octal D-type register configured to enable multiplexed transmission of data from bus to bus or internal register to bus.

This bus transceiver features totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic level drive provides this device with the capability of being connected directly to and driving the bus lines in a bus-organized system without the need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the DM74ALS646 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input bus data is stored into the appropriate register. The CAB input controls the transfer of data into the A register and the CBA input controls the B register.

The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A LOW input level selects real-time data, and a HIGH level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between store and real-time data.

The enable $\overline{G}$ and direction control pins provide four modes of operation: real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internally stored data transfer to bus A or B.

When the enable $\overline{G}$ pin is LOW, the direction pin selects which bus receives data. When the enable G pin is HIGH, both buses become disabled yet their input function is still enabled.

Features

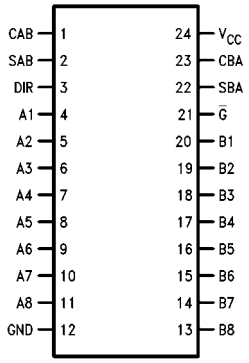
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- 3-STATE buffer outputs drive bus lines directly
- Multiplexed real-time and stored data
- Independent registers for A and B buses

Ordering Code

Order Number	Package Number	Package Description
DM74ALS646WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
DM74ALS646NT	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



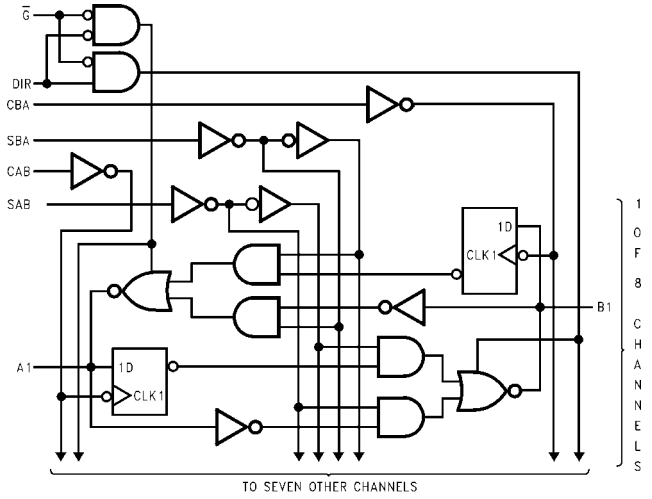
Function Table

Inputs						Data I/O (Note 1)		Operation or Function
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	
X	X	↑	X	X	X	Input	Not Specified	Store A, B Unspecified
X	X	X	↑	X	X	Not Specified	Input	Store B, A Unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H/L	H/L	X	X	Input	Input	Isolation, Hold Storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to a Bus
L	L	X	H/L	X	H	Output	Input	Stored B Data to a Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H/L	X	H	X	Input	Output	Stored A Data to B Bus

H = HIGH Logic Level
L = LOW Logic Level
X = Don't Care (Either LOW or HIGH Logic Levels including transitions)
H/L = Either LOW or HIGH Logic Level excluding transitions
↑ = Positive going edge of pulse

Note 1: The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

Logic Diagram



Absolute Maximum Ratings(Note 2)

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	44.5°C/W
M Package	80.5°C/W

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage		5	5.5	V
V_{IH}	HIGH Level Input Voltage				V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−15	mA
I_{OL}	LOW Level Output Current			24	mA
f_{CLK}	Clock Frequency			40	MHz
t_W	Pulse Duration, Clocks LOW or HIGH				ns
t_{SU}	Data Setup Time, A before CAB or B before CBA (Note 3)	10↑			ns
t_H	Data Hold Time, A after CAB or B after CBA (Note 3)	0↑			ns
T_A	Free Air Operating Temperature			70	°C

Note 3: ↑ = With reference to the LOW-to-HIGH transition of the respective clock.

Electrical Characteristics

over recommended free air temperature range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V
		V_{CC} = Min	I_{OH} = −3 mA	2.4	3.2		
			I_{OH} = Max	2			
V_{OL}	LOW Level Output Voltage	V_{CC} = Min	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
			I_{OL} = 48 mA		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	I/O Ports, V_I = 5.5V			100	μA
			Control Inputs, V_I = 7V			100	
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 4)				20	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max,	Control Inputs			−200	μA
		V_I = 0.4V, (Note 4)	I/O Ports			−200	
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs HIGH		47	76	mA
			Outputs LOW		55	88	
			Outputs Disabled		55	88	

Note 4: For I/O ports the 3-STATE output currents (I_{OZH} and I_{OZL}) are included in the I_{IH} and I_{IL} parameters.

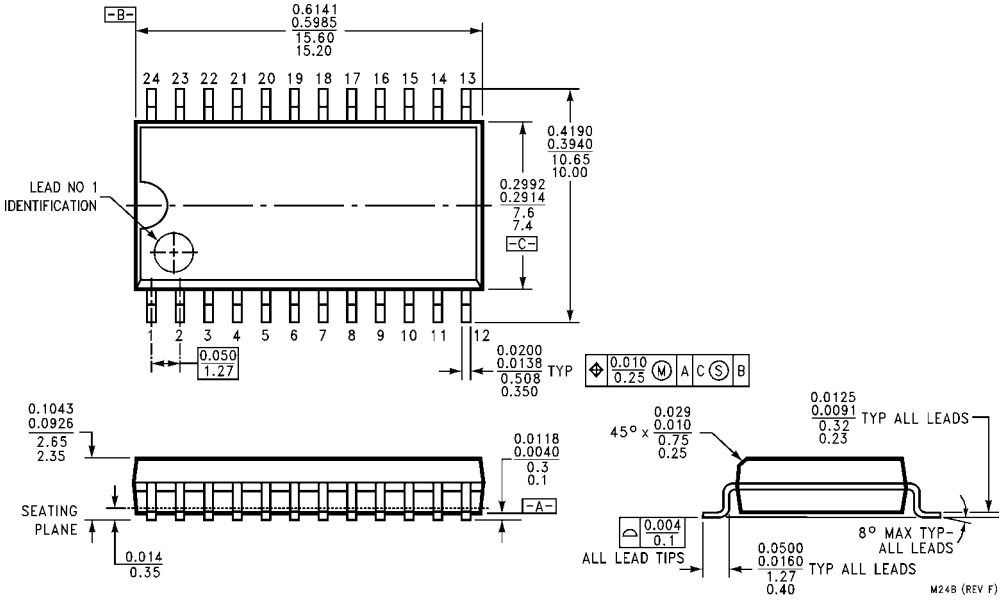
Switching Characteristics

over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, $R_1 = R_2$ = 500Ω, T_A = Min to Max	CBA or CAB to A or B	10	30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		CBA or CAB to A or B	5	17	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		A or B to B or A	5	20	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		A or B to B or A	3	12	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output (with A or B LOW) (Note 5)		SBA or SAB to A or B	12	35	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output (with A or B LOW) (Note 5)		SBA or SAB to A or B	5	20	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output (with A or B HIGH) (Note 5)		SBA or SAB to A or B	6	25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output (with A or B HIGH) (Note 5)		SBA or SAB to A or B	5	20	ns
t_{PZH}	Output Enable Time to HIGH Level Output		$\overline{G}$ to A or B	3	17	ns
t_{PZL}	Output Enable Time to LOW Level Output		$\overline{G}$ to A or B	5	20	ns
t_{PHZ}	Output Disable Time from HIGH Level Output		$\overline{G}$ to A or B	1	10	ns
t_{PLZ}	Output Disable Time from LOW Level Output		$\overline{G}$ to A or B	2	16	ns
t_{PZH}	Output Enable Time to HIGH Level Output		DIR to A or B	6	30	ns
t_{PZL}	Output Enable Time to LOW Level Output		DIR to A or B	5	25	ns
t_{PHZ}	Output Disable Time from HIGH Level Output		DIR to A or B	1	10	ns
t_{PLZ}	Output Disable Time from LOW Level Output		DIR to A or B	2	16	ns

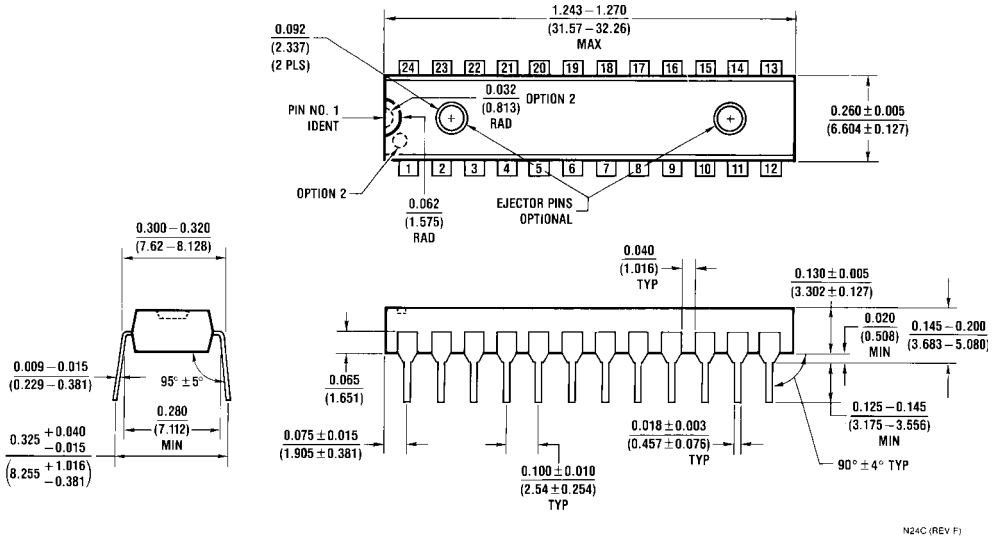
Note 5: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N24C

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com